Multiple Choice Questions

1. Intel 8085 is a _____ bit microprocessor.
   a) 4 bit b) **8 bit** c) 16 bit d) 32 bit
2. The time for the clock cycle of the Intel 8085 AH-2, version is _____
   a) 50 ns b) 100 ns c) 150 ns d) **200 ns**
3. The microprocessor 8085 has _____ basic instructions and _____ opcodes.
   a) **80, 246** b) 70, 346 c) 80, 346 d) 70, 246
4. _____ is flip-flop which indicates some condition which arises after the execution of an arithmetic or logic instruction.
   a) Instruction register b) Temporary register c) Status flag d) None of these
5. The number of status flags in 8085 are
   a) **5** b) 6 c) 8 d) 9
6. In 8085 name the 16 bit registers.
   (a) Stack Pointer (b) Program Counter (c)IR (d) **a and b**
7. Which stack in 8085?
   a) FIFO b) **LIFO** c) FILO d)LILO
8. What does mp speed depends on
   a) Clock b) Data bus width c) **Address bus width** d)Size of register
9. In8085 are of the following statements is not true
   a) Co processor is interfaced in max mode b) **Co processor is interfaced in min mode**
   c) Co processor is interfaced in max/min mode d) Supports pipelinig
10. The status that cannot be operated by direct instructions is
    a) Cy b) Z c) P d) **AC**
11. _____ and _____ are treated as a 16 bit unit for stack operation.
    a) **PSW and ACC** b) CS and P c) Z and S d) PC and SP
12. The width of address bus and data bus in 8085 are respectively ….
    a) **16, 8** b) 8,16 c) 8,8 d) 16,16
13. _____ memory locations can be addressed directly by Intel 8085.
    a) 34 K b) 44K c) 54 K d) **64 K**
14. The number of software interrupts in 8085 is ____
    a) 5 b) **8** c) 9 d) 10
15. Identify the non makeable interrupt in the following
    a) **RST4.5** b) RST5.5 c) RST6.5 d) RST 7.5
16. In response to RST 7.5 interrupt, the execution of control transfers to memory location...
    a) 0000H b) 002CH c) 0034H d) **003CH**
17. Which of following is both level and edge sensitive?
    a) RST 7.5 b) RST 5.5 c) **TRAP** d) INTR
18. The interrupt vector address for TRAP is
    a) 0000H b) **0024H** c) 0018H d) 002CH
19. The status of S0 and S1 pins for memory read is.
    a) 0, 0 b) 0,1 c) 1,0 d) **1,1**

20. The execution of RST n instruction causes the stack pointer to _____
    a) Incremented by two b) **decremented by two**
    c) remain unaffected d) none of the above
21. PSW stands for contents of _____
    a) Accumulator b) flag register c) **both of above** d) none of the two
22. Which interrupts has highest Priority
    a) INTR b) **TRAP** c) RST 7.5 d)RST6.5
23. What is RST for the TRAP
    a) RST5.5 (b) **RST4.5** c) RST4 d)RST 5
24. Which of the following is a hardware interrupt.
    a) RST 5.5 ,RST 6.5 ,RST 7.5 b) INTR ,TRAP c)TRAP d) **a and b**
25. What are level triggering interrupts
    a) **RST 6.5 and RST5.5** b) RST7.5 and RST 6.5 c) RST 5.5 and RST7.5 d) INTR and TRAP
26. What is SIM?
    a) Select interrupt mask b) Sorting interrupt mask
    c) **Set interrupt mask** d) Softer interrupt mask
27. What is software interrupt?
    a) **RSTO-7** b) RST5.5 -RST 7.5 c)INTR d)TRAP
28. RIM is used to check whether----------?
    a) the write operation is done or not. b) t**he interrupt is masked or not.**
    c) the read operation is done or not. d) a&b
29. In 8085, example for non maskable interrupts is
    a) **TRAP** b) RST 6.5 c) INTR d) RST 5.5
30. Address line for RST 3 is
    a) 0020H b) 0028H c) **0018H** d) 0038H
31. The second part of the instruction is the data to be operated on, and it is called _____
    a) opcode b) **operand** c) instruction cycle d) fetch cycle
32. The first part of an instruction which specifies the task to be performed by the computer is called _____
    a) **opcode** b) operand c) instruction cycle d) fetch cycle
33. Which of the following is a one-byte instruction?
    a) MVI B, 05 b) LDA 2500H c) IN 01 d) **MOV A,B**
34. Which of the following is a two-byte instruction?
    a) MVI B, 05 b) LDA 2500H c) IN 01 d) **both a and c**
35. The necessary steps carried out to perform the operation of accessing either memory or I/O Device, constitute a _____
    a) fetch operation b) execute operation c) **machine cycle** d) instruction cycle
36. The status of S0 and S1 pins for memory write is.
    a) 0, 0 b) 0,1 c) **1,0** d) 1,1

37. The status of S0 and S1 pins for memory fetch is.
    a) 0, 0 b) 0, 1 c) 1,0 d) **1,1**
38. The interrupt vector address for RST 6.5 is
    a) 0000H b) **0034H** c) 0018H d) 002CH
39. The interrupt vector address for RST 5.5 is
    a) 0000H b) 0034H c) 0018H d) **002CH**
40. The difference between memory and storage is that the memory is_____ and storage is_____
    a) **Temporary, permanent** b) Permanent, temporary c) Slow, fast d) None of the above
41. Which of the Following holds the ROM, CPU, RAM and expansion cards?
    a) Hard disk b) Floppy disk c) **Mother board** d) None of the above
42. The language that the computer can understand and execute is called _____
    a) **Machine language** b) Application software c) System program d) None of the above
43. Actual execution of instructions in a computer takes place in
    a) **ALU** b) Control Unit c) Storage unit d) None of the above
44. Execution of two or more programs by a single CPU is known as:
    a) Multiprocessing b) Time sharing c) **Multiprogramming** d) None of the above
45. Operating system is_____
    a) A collection of hardware components c) **A collection of software routines**
    b) A collection of input-output devices d) none of the above
46. The part of machine level instruction, which tells the central processor what was to be done is
    a) **Operation code** b) Address c) Operand d) None of the above
47. The communication line between the CPU, memory and peripherals is called a
    a) **Bus** b) line c) media d) none of these
48. The language that the computer can understand and execute is called
    a) **Machine language** b) Application software c) System program d) None of the above
49. A step by step procedure used to solve a problem is called
    a)Operating system b) **Algorithm** c) Application Program d) None of the above
50. The Central Processing Unit:
    a) is operated from the control panel. b) is controlled by the input data entering the system
    c) controls the auxiliary storage unit d) **controls all input, output and processing.**
51. C is
    a) An assembly language b) **A third generation high level language**
    c) A machine language d) None of the above
52. In 1st Complement a number which is Subtracted from other number is known as…….
    a) Carry b) subtrahend c) **minuend** d) Non of this
53. In a 2nd Complement a number which is subtracted from other number is known as……..
    a) Carry b) **Subtrahend** c) Minuend d) Non of this
54. In 2nd Complement a number which is subtracted from other number is known as……..
    a) Carry b) Subtrahend c**) Minuend** d) None of them
55. 8085 was introduced in _____

a) 1971 b) **1976** c) 1972 d) 1978

56. The First Microprocessor was_____
    a) **Intel 4004** b) 8080 c) 8085 d) 4008
57. Which is a 8 bit Microprocessor _____
    a) Intel 4040 b) Pentium – I c) 8088 d) **Motorala MC-6801**
58. Pentium-I, Pentium-II, Pentium-III and Pentium-IV are recently introduced microprocessor by_____
    a) Motorala b) **Intel** c) Stephen Mors d) None
59. The address bus flow in _____
    a) bidirection b) **unidirection** c) Mulidirection d) Circular
60. Status register is also called as _____
    a) Accumulator b) Stack c) Counter d) **flags**
61. The 8085 is based in a _____ pin DIP
    a) **40** b) 45 c) 20 d) 35
62. The 8085 Microprocessor uses_____ V power supply
    a) **+5V** b) -5V c) +12v d) -12v
63. The address / data bus in 8085 is _____
    a) **Multiplexed** b) demultiplexed c) decoded d) loaded
64. The Device which converts instructions into the binary form that is understood by the computer and supply to the computer is known as_____
    a) **Input** b) Output c) Automatic d) Memory
65. Can ROM be used as stack?
    a) Yes b) **No** c) Some times yes d) Some times no
66. The advantage of memory mapped i/o over i/o mapped i/o is _____
    a) Faster b) Many instructions supporting memory mapped i/o
    c) Require a bigger address decoder d) **All of the above.**
67. If the contents of SP are 1000H, the content of B and C registers after PUSH B instruction are...
    a) **0FFFH, OFFEH** b) 0FFE H ,0FFF c) 1000 H,0FFF H d) 1000 H, 1001H
68. In an 8085 system, let SP=2000 H. Then after execution of POP H instruction will transfer the memory contents as…
    a) 2001H and 2002H to H and L register b) **2001H and 2000H in to H and L registers**
    c) 2000H and 1FFFH to H and L registers d) 2000H and 1999H to H and L registers
69. Let contents of accumulator and B are 00000100 and 01000000 respectively. After execution of SUB B instruction, accumulator contents are….
    a) 00000100 b) 01000000 c) **11000100** d) 010001000
70. Let the contents of C register be 00000000. The contents of C register after execution of DCR C is _____
    a) 00000000 b) **11111111** c) 00000001 d) none of above
71. In an 8085 based system, the maximum number of input output devices can be connected using I/0 mapped I/O method is
    a) 64 b) **512** c) 256 d) 65536

72. After the execution of CMA instruction, the status of Z and Cy flags are respectively
    a) **set, reset** b) set, unchanged c) reset, set d)reset, unchanged
73. The 8085 will enter in to INA cycle after the execution of…
    a) any interrupt b)TRAP only c) **INTR only** d) RST 7.5,6.5,5.5 only
74. To reset carry without affecting accumulator contents, we have to use
    a) SUB A b) XRA A c) **ORA A** d) CMC
75. In order to complement the lower order nibble of the accumulator, we can use …
    a) ANI 0FH b) **XRI 0FH** c) ORI 0FH d) CMA
76. Which of the following instruction will never affect the zero flag..
    a)DCR reg b) ORA reg c) **DCX rp** d) XRA reg
77. The interface peripheral used with key board is
    a) 8251 b) **8279** c) 8259 d) 8253
78. To save accumulator value on to the stack, which of the following instructions may be used..
    a) **PUSH PSW** b) PUSH A c) PUSH SP d) POP PSW
79. A single instruction to clear the lower 4 bits of accumulator in 8085 alp is…….
    a) XRI 0FH b) **ANI F0 H** c) XRI F0H d)ANI 0FH
80. Interfacing devices for DMA controller, programmable interval timer are respectively…
    a) **8257, 8253** b) 8253, 8257 c) 8257,8251 d)8251,8257
81. If the contents of register B are greater than that of accumulator, CMP B will affect carry flag, zero flag respectively as..
    a) **set, reset** b) reset, set c) reset, reset d) set, set
82. The status of s, z, cy flags after execution of following instructions are……
    MVI A, A9H
    MVI B, 57H
    ADD B
    ORA A
    a) 0,1,1 b)**0,1,0** c)1,0,0 d)1,0,1
83. The contents of registers A and B after execution of following instructions are..
    XRA A
    MVI B, 4AH
    SUI 4FH
    ANA B
    HLT
    a) 05,4A b) 4F, 00 c) B1, 4A d) **00,4A**
84. The instruction that does not clear the contents of accumulator of 8085 is..
    a) XRA A b) ANI 00H c) MVI A,00H d) **none of them**
85. The loop will be executed after the following instructions…
    XRA A
    LXI B, 0007H
    LOOP: DCX B

JNZ LOOP

a) **1 time** b) 8 times c) 7times d) infinite times

86. Consider the loop

LXI H, 000AH

LOOP: DCX B

MOV A, B

ORA C

JNZ LOOP

This loop will be executed by

a) 1 time b) **10 times** c)11 times d) infinite times

87. The contents of accumulator after the execution of following instructions will be

MVI A, B7H

ORA A

RAL

a) 6EH b) **4FH** c) EEH d)EFH

88. The contents of the accumulator after execution of following instructions

MVI A, 07H

RLC

MOV B, A

RLC

RLC

ADD B

a) **46H** b)70H c)38H d)68H

89. If the accumulator of 8085 contains 37H and the previous operation has set the carry flag, the instruction ACI 56H will result in

a) 8DH b) **8EH** c) 17H d) 18H

90. Consider the execution of the following instruction by 8085.

MVI H, 01FFH

SHLD 2050H

After execution the contents of memory loction 2050H,2051H and registers H,L will be respectively…

a) 00H,01H,FFH,FFH b) FFH,01H,FFH,01H

c) **FFH,01H,01H,FFH** d) 01H,FFH,FFH,FFH

91. Consider the following set of 8085 instruction.

MVI A,82H

ORA A

JP DSPLY

XRA A

DSPLY:OUT PORT1

HLT.

The output at PORT1 is

a) **00H** b) FFH c) 92H d) 11H

92. After the execution of following instructions, contents of PC and HL are…

    LXI H, 30A0
    DAD H
    PCHL

    a) PC=2715H HL=30A0H b) PC=30A0H, HL=2715H
    c) **PC-6140H, HL=6140H** d) PC=6140H, HL=2715H

93. If the following program starts at 0100H, the contents of accumulator when PC reaches 0109H _____

    LXI SP, 00FFH
    LXI H, 0107H
    MVI A, 20H
    SUB M

    a) 20H b) 02H c) **00H** d) FFH

94. Let the contents of B register and accumulator are 49h and 3AH respectively. The contents of accumulator, status of carry flag and sign flag are..

    a) **F1H,1,1** b) 0F,1,1 c) F0H,0,0 d) 1FH,1,1

95. The contents of SP, HL after the execution of following instructions.

    LXI SP, 27FF
    CALL 1006
    POP H

    a) 27FF,1003 b) 27FD,1003 c) **27FF,1006** d) 27FD,1006

96. The contents of accumulator after the execution of following set of instructions is

    XRA A
    MVI B, F0H
    SUB B

    a) 01H b) 0FH c)F0H d)**10H**

97. The instruction used for storing the contents of H and L registers in to 2050H and 2051h respectively is...

    a) SPHL 2050H b)SPHL2051H c) **SHLD 2050 H** d) STAX 2050 H

98. The number of times that the NOP operation executed in the following program is..

    MVI A, 10H
    MVI B, 10H
    BACK: NOP
    ADD B
    RLC
    JNC BACK
    HLT

    a) 1 b) 2 c) **3** d) 4

99. After the execution of XRA A instruction

    a) CY flag set b) CY flag is reset c) **Z flag is set** d) Z flag is reset

100. An m-bit microprcessohas m-bit
    a) Flag register b) data registers c) **program counter** d) instruction register
101. If the contents of SP and PC are F000H and 2400H. The contents after CALL E000 will be
    a) PC:F003 SP:2400 b) PC:E000M SP:2400
    c) **PC:E000,SP:EFFE** d) PC:E000,SP:23FE
102. The SIM instruction outputs the contents of accumulator to define …
    a) interrupt mask bit b) serial output data line c) **both above** d) none of them
103. The content of flag register after the following set of instructions are executed…
    LXI SP,209FH
    MVI C,00H
    PUSH B
    POP PSW
    RET
    a)10H b)20H c)**00H** d)9F
104. The contents of accumulator after the execution of the following set of instructions.
    MVI A,30H
    ACI 30H
    XRA A
    POP H
    a) 30H b) 60H c) **00H** d) contents of stack memory
105. The content of accumulator before CMA instruction is A5H. Its content after instruction execution is
    a) A5H b) **5AH** c) AAH d) 55H

Two Marks Questions

1. **Which type of architecture 8085 has?**
   8085 has Von Neumann architecture. It was derived after the name of mathematician John Von Neumann. Its having 16 address bus and 8 bit data bus.it can access 2^16 individual memory location.
2. **How many memory locations can be addressed by a microprocessor with 14 address lines?**
   2^14=16384
3. **8085 is how many bit microprocessor?**
   8 bit as its data bus is 8 bit.
4. **Why is data bus bi-directional?**
   As it has to carry data from mp to external device or the reverse.
5. **What is the function of accumulator?**
   This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator.
6. **What is flag?**

The ALU includes five flip-flops, which are set or reset after an operation according to data conditions of the result in the accumulator and other registers. They are called Zero(Z), Carry (CY), Sign (S), Parity (P), and Auxiliary Carry (AC) flags.

7. **What is bus?**

   Typical system uses a number of busses, collection of wires, which transmit binary numbers, one bit per wire. A typical microprocessor communicates with memory and other devices (input and output) using three busses: Address Bus, Data Bus and Control Bus.

8. **What is the role of Address Bus?**

   The Address Bus consists of 16 wires, therefore Its "width" is 16 bits. A 16 bit Address bus can identify 2^16=65536 memory locations i.e. 0000000000000000 up to 1111111111111111. Because memory consists of boxes, each with a unique address, the size of the address bus determines the size of memory, which can be used. To communicate with memory the microprocessor sends an address on the address bus, eg 0000000000000011 (3 in decimal), to the memory. The memory the selects box number 3 for reading or writing data. Address bus is unidirectional, ie numbers only sent from microprocessor to memory, not other way.

9. **What is the role of Data Bus?**

   Data Bus: carries .8-bit data., in binary form, between ìP and other external units, such as memory. The Data Bus typically consists of 8 wires. Data bus used to transmit "data", i.e. information, results of arithmetic, etc, between memory and ìP. Bus is bi-directional. Size of the data bus determines what arithmetic can be done. If only 8 bits wide then largest number is 11111111 (255 in decimal). Data Bus also carries instructions from memory to the microprocessor. Size of the bus therefore limits the number of possible instructions to 256, each specified by a separate number.

10. **What is the role of Control Bus?**

    It is a group of various single lines used to provide control and synchronization signals. ìP generates different control signals for different operations. These signals are used to identify the device with which the ìP wants to communicate.

11. **What are tri-state devices and why they are essential in a bus oriented system?**

    Tri state logic devices have three states (0, 1 and high impedance). When the enable (may be active high or active low) line is activated, the device works. The disabled enable line makes the device at high impedance state and it is disconnected from the circuit.
    In microcomputer system the peripherals are connected in parallel between address bus and data bus. Because of tri stated interfacing devices, peripherals do not load the system buses. Processor communicates with one peripheral or device at a time by enabling the tri state line of the interfacing peripheral or device. Tri state logic is critical to proper functioning of the microcomputer.

12. **Why are program counter and stack pointer 16-bit registers?**

    Because SP points to the beginning of stack memory (LXI SP 8000H) which is 16-bits.
    Also PC points to the memory locations (16-bits) of the instructions to be excecuted to maintain the proper sequence of execution of program.

13. What are the different addressing modes in 8085?

Register:-

Data is provided through the registers. Or operand is only register(s). Example: MOV Rd, Rs.

Register indirect:-

Operand M or register pair. Example: MOV A,M; LDAX B; STAX D; MVI M,32H (exception for immediate addressing mode).

Direct:-

Operand 8-bit port address or 16-bit memory address. Example: IN 84H, OUT 84H, all CALLs.

Immediate:-

Instruction having the letter I. Or immediate data to the destination provided. Also all jump instructions as the meaning is jump immediately. Example MVI M, 2H; ADI 47H; LXIH 2050 (exception for direct addressing mode).

Implicit:-

No operand. Example: XCHG.

14. What is the difference between MOV and MVI?

Opcode	Operand	Bytes	M-cycles	T-states
MOV	Rd, Rs, M, Rs, Rd, M	1	1 2 2	4 7 7
MVI	reg, data M, data	2 2	2 3	7 10

Rd = Destination register, Rs = Source register, M =Memory location pointed out by HL register pair, reg =Regiser, data = 8-bit data.

15. What happens during DMA transfer?

To make a fast data transfer, the MPU releases the control of its buses to DMA. DMA acts as an external device and the active high input signal HOLD goes HIGH when the DMA is requesting to the MPU to use its buses. After receiving the HOLD request from DMA, the MPU releases the buses in the following machine cycle and generates an active high output signal HLDA indicating the release of buses. Once the DMA gains that control, it acts in the role of the MPU for data transfer.

16. What is PSW?

PSW (Program Status Word) represents the contents of the accumulator and the flag register together considering the accumulator as the high order and flag as the low order register as if it is the AF register pair. For example POP PSW.

17. What is ALE? Explain the functions of ALE in 8085.

It is the acronym for Address Latch Enable (pin number 30) used to demultiplex the multiplexed lower order address/data bus. During T1 the ALE goes HIGH. When ALE goes HIGH, the latch is enabled. So the o/p changes according to the i/p data. During T1 the o/p of latch is 05H. When

ALE goes LOW, the data byte 05H is latched until the next ALE. And after the latching operation the o/p of the latch represents the lower order address bus A0-A7.

18. **Which line will be activated when an output device require attention from CPU?**
    Interrupt Request (INTR, pin 10, it is an input signal to ìP). It goes high when the external devices want to communicate.
19. **Can an RC circuit be used as clock source for 8085?**
    Yes, it can be used, if an accurate clock frequency is not required. Also, the component cost is low compared to LC or Crystal.
20. **Which interrupt is not level-sensitive in 8085?**
    RST 7.5 is a raising edge-triggering interrupt.
21. **What does Quality factor mean?**
    The Quality factor is also defined, as Q. So it is a number, which reflects the lossness of a circuit. Higher the Q, the lower are the losses.
22. **What are level-triggering interrupt?**
    RST 6.5 & RST 5.5 are level-triggering interrupts.
23. **Comparison between full address decoding and partial address decoding?**

Full Address Decoding	Partial Address decoding
1. All higher address lines are decoded to select the memory or I/O device.	1. Few higher address lines are decoded to select the memory or I/O device.
2. More hardware is required to design decoding logic.	2. Hardware required to design decoding logic is less and sometimes it can be eliminated.
3. Higher cost for decoding circuit.	3. Less cost for decoding circuit.
4. No Multiple addresses.	4. It has a advantage of multiple addresses.
5. Used in large systems	5. Used in small systems

24. **Give some examples of port devices used in 8085 microprocessor based system?**
    The various port devices used in 8085 are 8212,8155,8156,8255,8355,8755.

25. **What is the need for timing diagram?**
    The timing diagram provides information regarding the status of various signals, when a machine cycle is executed. The knowledge of timing diagram is essential for system designer to select matched peripheral devices like memories, latches, ports etc from a microprocessor system.

26. **22. What is vectored and non-vectored interrupt?**

When an interrupt is accepted, if the processor control branches to a specific address defined by the manufacturer then the interrupt is called vectored interrupt. In Non-vectored interrupt there is no specific address for storing the interrupt service routine. Hence the interrupted device should give the address of the interrupt service routine.

27. When the 8085 processor checks for an interrupt?

In the second T-state of the last machine cycle of every instruction, the 8085 processor checks whether an interrupt request is made or not.

28. What is a port?

The port is a buffered I/O, which is used to hold the data transmitted from the microprocessor to I/O devices and vice versa.

29. Advantages of differential data transfer?

1. Communication at high data rate in real world environment.
2. Differential data transmission offers superior performance.
3. Differential signals can help induced noise signals.

30. What are the types of rotate instructions?

RLC – Rotate Accumulator Left
RRC- Rotate Accumulator Right
RAL – Rotate Accumulator Left through Carry
RAR - Rotate Accumulator Right through Carry

31. What are the operating modes of 8255?

1. Bit set/Reset mode
2. I/O modes
    a)mode 0 : Simple input/output
    b)mode 1 : Input/output with handshake
    c)mode 2 : Bi-directional I/O data transfer

32. What is Microprocessor? Give the power supply & clock frequency of 8085?

A microprocessor is a multipurpose, programmable logic device that reads binary instructions from a storage device called memory accepts binary data as input and processes data according to those instructions and provides result as output. The power supply of 8085 is +5V and clock frequency in 3MHz.

33. List few applications of microprocessor-based system.

It is used:

i. For measurements, display and control of current, voltage, temperature, pressure, etc.
ii. For traffic control and industrial tool control.
iii. For speed control of machines.

34. What are the functions of an accumulator?

The accumulator is the register associated with the ALU operations and sometimes I/O operations. It is an integral part of ALU. It holds one of data to be processed by ALU. It also temporarily stores the result of the operation performed by the ALU.

35. List the 16 – bit registers of 8085 microprocessor.

Stack pointer (SP) and Program counter (PC).

36. List the allowed register pairs of 8085.

* B-C register pair
* D-E register pair
* H-L register pair

37. What is a microcomputer?

A computer that is designed using a microprocessor as its CPU is called microcomputer.

38. What is the signal classification of 8085?

All the signals of 8085 can be classified into 6 groups

- Address bus
- Data bus
- Control and status signals
- Power supply and frequency signals
- Externally initiated signals
- Serial I/O ports

39. What are operations performed on data in 8085?

The various operations performed are

* Store 8-bit data
* Perform arithmetic and logical operations
* Test for conditions
* Sequence the execution of instructions
* Store data temporarily during execution in the defined R/W memory locations called the stack

40. Steps involved to fetch a byte in 8085

i. The PC places the 16-bit memory address on the address bus

ii. The control unit sends the control signal RD to enable the memory chip

iii. The byte from the memory location is placed on the data bus

iv. The byte is placed in the instruction decoder of the microprocessor and the task is carried out according to the instruction.

41. Define instruction cycle, machine cycle and T-state

Instruction cycle is defined, as the time required completing the execution of an instruction. Machine cycle is defined as the time required completing one operation of accessing memory, I/O or acknowledging an external request. Tcycle is defined as one subdivision of the operation performed in one clock period.

42. What is an instruction?

An instruction is a binary pattern entered through an input device to command the microprocessor to perform that specific function.

43. What is the use of ALE?

The ALE is used to latch the lower order address so that it can be available in T2 and T3 and used for identifying the memory address. During T1 the ALE goes high, the latch is transparent ie, the

output changes according to the input data, so the output of the latch is the lower order address. When ALE goes low the lower order address is latched until the next ALE.

44. How many machine cycles does 8085 have, mention them?

The 8085 have seven machine cycles. They are

- Opcode fetch
- Memory read
- Memory write
- I/O read
- I/O write
- Interrupt acknowledge
- Bus idle

45. Explain the signals HOLD, READY and SID.

HOLD indicates that a peripheral such as DMA controller is requesting the use of address bus, data bus and control bus. READY is used to delay the microprocessor read or write cycles until a slow responding peripheral is ready to send or accept data.SID is used to accept serial data bit by bit.

46. Mention the categories of instruction and give two examples for each category.

The instructions of 8085 can be categorized into the following five categories

- Data transfer Instructions -MOV Rd,Rs STA 16-bit
- Arithmetic Instructions -ADD R DCR M
- Logical Instructions -XRI 8-bit RAR
- Branching Instructions -JNZ CALL 16-bit
- Machine control Instructions -HLT NOP

47. Explain LDA, STA and DAA instructions.

LDA copies the data byte into accumulator from the memory location specified by the 16-bit address. STA copies the data byte from the accumulator in the memory location specified by 16-bit address. DAA changes the contents of the accumulator from binary to 4-bit BCD digits.

48. Explain the different instruction formats with examples.

The instruction set is grouped into the following formats

- One byte instruction -MOV C,A
- Two byte instruction -MVI A,39H
- Three byte instruction -JMP 2345H

49. What is the use of addressing modes, mention the different types?

The various formats of specifying the operands are called addressing modes, it is used to access the operands or data. The different types are as follows

- Immediate addressing
- Register addressing
- Direct addressing
- Indirect addressing
- Implicit addressing

50. What is the use of bi-directional buffers?

It is used to increase the driving capacity of the data bus. The data bus of a microcomputer system is bi-directional, so it requires a buffer that allows the data to flow in both directions.

51. Give the register organization of 8085

W(8)	**Temp. Reg**
Z(8)	**Temp. Reg**
B(8)	**Register**
C(8)	**Register**
D(8)	**Register**
E(8)	**Register**
H(8)	**Register**
L(8)	**Register**
Stack Pointer	**(16)**
Program Counter	**(16)**

52. Define stack and explain stack related instructions.

The stack is a group of memory locations in the R/W memory that is used for the temporary storage of binary information during the execution of the program. The stack related instructions are PUSH & POP.

53. Why do we use XRA A instruction

The XRA A instruction is used to clear the contents of the Accumulator and store the value 00H.

54. Compare CALL and PUSH instructions

CALL	PUSH
1.When CALL is executed the microprocessor automatically stores the 16-bit address of the instruction next to CALL on the stack. **2.When CALL is executed the stack pointer is decremented by two**	**1.PUSH The programmer uses the instruction to save the contents of the register pair on the stack** **2. When PUSH is executed the stack pointer is decremented by two**

55. What is Microcontroller and Microcomputer?`

Microcontroller is a device that includes microprocessor; memory and I/O signal lines on a single chip, fabricated using VLSI technology. Microcomputer is a computer that is designed using microprocessor as its CPU. It includes microprocessor, memory and I/O.

56. Define Flags.

The flags are used to reflect the data conditions in the accumulator. The 8085 flags are S-Sign flag, Z-Zero flag, AC-Auxiliary carry flag, P-Parity flag, CY Carry flag, D7 D6 D5 D4 D3 D2 D1 D0.

57. How does the microprocessor differentiate between data and instruction?

When the first m/c code of an instruction is fetched and decoded in the instruction register, the microprocessor recognizes the number of bytes required to fetch the entire instruction. For

example MVI A, Data, the second byte is always considered as data. If the data byte is omitted by mistake whatever is in that memory location will be considered as data & the byte after the "data" will be treated as the next instruction.

58. Compare RET and POP.

RET	POP
1.RET transfers the contents of the top two locations of the stack to the PC 2.When RET is executed the SP is incremented by two 3.Has 8 conditional RETURN instructions	1.POP transfers the contents of the top two locations of the stack to the specified register pair 2. When POP is executed the SP is incremented by two 3.No conditional POP instructions

59. What is assembler?

The assembler translates the assembly language program text which is given as input to the assembler to their binary equivalents known as object code. The time required to translate the assembly code to object code is called access time. The assembler checks for syntax errors & displays them before giving the object code.

60. What is loader?

The loader copies the program into the computer's main memory at load time and begins the program execution at execution time.

61. What is linker?

A linker is a program used to join together several object files into one large object file. For large programs it is more efficient to divide the large program modules into smaller modules. Each module is individually written, tested & debugged. When all the modules work they are linked together to form a large functioning program.

62. What is interrupt service routine?

Interrupt means to break the sequence of operation. While the CPU is executing a program an interrupt breaks the normal sequence of execution of instructions & diverts its execution to some other program. This program to which the control is transferred is called the interrupt service routine.

63. What are the various programmed data transfer methods?

i) Synchronous data transfer
ii) Asynchronous data transfer
iii) Interrupt driven data transfer

64. What is interfacing?

An interface is a shared boundary between the devices which involves sharing information. Interfacing is the process of making two different systems communicate with each other.

65. List the operation modes of 8255

a. I.O Mode
   i.Mode 0-Simple Input/Output.
   ii. Mode 1-Strobed Input/Output (Handshake mode)
   iii. Mode 2-Strobed bidirectional mode

b) Bit Set/Reset Mode.

66. What is a control word?

It is a word stored in a register (control register) used to control the operation of a program digital device.

67. What is the function of DMA address register?

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. Thus the starting address of the memory block that will be accessed by the device is first loaded in the DMA address register of the channel. Naturally, the device that wants to transfer data over a DMA channel, will access the block of memory with the starting address stored in the DMA Address Register.

68. What is the purpose of control word written to control register in 8255?

The control words written to control register specify an I/O function for each I.O port. The bit D7 of the control word determines either the I/O function of the BSR function.

69. What is the size of ports in 8255?

Port-A : 8-bits
Port-B : 8-bits
Port-CU : 4-bits
Port-CL : 4-bits

70. Difference between memory mapped I/o and I/O mapped I/o?

Memory Mapped I/O	I/O mapped I/o
In this device address is 16- bit. Thus Ao to A15 lines are used to generate the device address	In this device address is 8-bit. Thus Ao to A7 or A8 to A15 lines are used to generate device address.
MEMR and MEMW control signals are used to control read and write I/O operations.	IOR and IOW control signals are used to control read and write I/O operations.
Instructions available are LDA,STA,MOV R,M , ADD M etc	Instructions available are IN and OUT.
Data transfer is between any register and I/O device.	Data transfer is between accumulator and I/O device.
Decoding 16-bit address may require more hardware.	Decoding 8-bit address will require less hardware.

71. Distinguish between the memories mapped I/O peripheral I/O?

Memory Mapped I/O	Peripheral MappedI/O
16-bit device address	8-bit device address
Data transfer between any general-purpose register and I/O port.	Data is transfer only between accumulator and I.O port
The memory map (64K) is shared between I/O device and system memory.	The I/O map is independent of the memory map; 256 input device and 256 output device can be connected
More hardware is required to decode 16-bit address	Less hardware is required to decode 8-bit address
Arithmetic or logic operation can be directly performed with I/O data	Arithmetic or logical operation cannot be directly performed with I/O data

72. What are memory mapping and I/O mapping?

Memory mapping:

The assignment of memory addresses to various registers in a memory chip is called as memory mapping.

I/O mapping:

The assignment of addresses to various I/O devices in the memory chip is called as I/O mapping.

73. What is status flag bit?

The flag register reflects the results of logical and arithmetic instructions. The flag register digits D0, D2, D4, D6, D7 and D11 are modified according to the result of the execution of logical and arithmetic instruction. These are called as status flag bits.

74. What is a control flag?

The bits D8 and D9 namely, trap flag (TF) and interrupt flag (IF) bits, are used for controlling machine operation and thus they are called control flags.

75. Compare Microprocessor and Microcontroller.

Microprocessor	Microcontroller
Microprocessor contains ALU, general purpose registers, stack pointer, program counter, clock timing circuit and interrupt circuit.	Microcontroller contains the circuitry of microprocessor and in addition it has built- in ROM, RAM, I/O devices, timers and counters.
It has many instructions to move data between memory and CPU.	It has one or two instructions to move data between memory and CPU.
It has one or two bit handling instructions.	It has many bit handling instructions.
Access times for memory and I/O devices are more.	Less access times for built-in memory and I/O devices.
Microprocessor based system requires more hardware.	Microcontroller based system requires less hardware reducing PCB size and increasing the

	reliability.

76. What are the various registers in 8085?

Accumulator register, Temporary register, Instruction register, Stack Pointer, Program Counter are the various registers in 8085 .

77. What are the various flags used in 8085?

Sign flag, Zero flag, Auxillary flag, Parity flag, Carry flag.

78. What is Stack Pointer?

Stack pointer is a special purpose 16-bit register in the Microprocessor, which holds the address of the top of the stack.

79. What is Program counter?

Program counter holds the address of either the first byte of the next instruction to be fetched for execution or the address of the next byte of a multi byte instruction, which has not been completely fetched. In both the cases it gets incremented automatically one by one as the instruction bytes get fetched. Also Program register keeps the address of the next instruction.

80. Which Stack is used in 8085?

LIFO (Last In First Out) stack is used in 8085.In this type of Stack the last stored information can be retrieved first.

81. What happens when HLT instruction is executed in processor?

The Micro Processor enters into Halt-State and the buses are tri-stated.

82. What is meant by a bus?

A bus is a group of conducting lines that carriers data, address, & control signals.

83. What is Tri-state logic?

Three Logic Levels are used and they are High, Low, High impedance state. The high and low are normal logic levels & high impedance state is electrical open circuit conditions. Tri-state logic has a third line called enable line.

84. Give an example of one address microprocessor?

8085a one address microprocessor.

85. In what way interrupts are classified in 8085?

In 8085 the interrupts are classified as Hardware and Software interrupts.

86. What are Hardware interrupts?

TRAP, RST7.5, RST6.5, RST5.5, INTR.

87. What are Software interrupts?

RST0, RST1, RST2, RST3, RST4, RST5, RST6, RST7.

88. Which interrupt has the highest priority?

TRAP has the highest priority.

89. Name 5 different addressing modes?

Immediate, Direct, Register, Register indirect, Implied addressing modes.

90. In 8085 which is called as High order / Low order Register?

Flag is called as Low order register & Accumulator is called as High order Register.

91. What are input & output devices?

Keyboards, Floppy disk are the examples of input devices. Printer, LED / LCD display, CRT Monitor are the examples of output devices.

92. Can an RC circuit be used as clock source for 8085?

Yes, it can be used, if an accurate clock frequency is not required. Also, the component cost is low compared to LC or Crystal.

93. Why crystal is a preferred clock source?

Because of high stability, large Q (Quality Factor) & the frequency that doesn't drift with aging. Crystal is used as a clock source most of the times.

94. Which interrupt is not level-sensitive in 8085?

RST 7.5 is a raising edge-triggering interrupt.

95. What does Quality factor mean?

The Quality factor is also defined, as Q. So it is a number, which reflects the lossness of a circuit. Higher the Q, the lower are the losses.

96. What are level-triggering interrupt?

Ans:- RST 6.5 & RST 5.5 are level-triggering interrupts.

97. What is meant by Maskable interrupts?

An interrupt that can be turned off by the programmer is known as Maskable interrupt.

98. What is Non-Maskable interrupts?

An interrupt which can be never be turned off (ie.disabled) is known as Non-Maskable interrupt.

99. Which interrupts are generally used for critical events?

Non-Maskable interrupts are used in critical events. Such as Power failure, Emergency, Shut off etc.,

100. Give examples for Maskable interrupts?

RST 7.5, RST6.5, RST5.5 are Maskable interrupts.

101. Give example for Non-Maskable interrupts?

Trap is known as Non-Maskable interrupts, which is used in emergency condition.

102. List out the five categories of the 8085 instructions. Give examples of the instructions for each group.

Data transfer group – MOV, MVI, LXI.

Arithmetic group – ADD, SUB, INR.

Logical group –ANA, XRA, CMP.

Branch group – JMP, JNZ, CALL.

Stack I/O and Machine control group – PUSH, POP, IN, HLT.

103. Explain the difference between a JMP instruction and CALL instruction.

A JMP instruction permanently changes the program counter. A CALL instruction leaves information on the stack so that the original program execution sequence can be resumed.

104. Explain the purpose of the I/O instructions IN and OUT.

The IN instruction is used to move data from an I/O port into the accumulator. The OUT instruction is used to move data from the accumulator to an I/O port. The IN & OUT instructions are used only on microprocessor, which use a separate address space for interfacing.

105. What is the difference between the shift and rotate instructions?

A rotate instruction is a closed loop instruction. That is, the data moved out at one end is put back in at the other end. The shift instruction loses the data that is moved out of the last bit locations.

106. How many address lines in a 4096 x 8 EPROM CHIP?

12 address lines.

107. What are the Control signals used for DMA operation?

HOLD & HLDA.

108. What do you mean by wait state? What is its need?

A wait state is a delay experienced by ìP when accessing external memory or another device that is slow to respond. the vice versa also cone into scenario. Now, to be able to access slow memory the ìP must be able to delay the transfer until the memory access is complete. One way is to increase the ìP clock period by reducing the clock frequency. Some ìPs provide a special control input called READY to allow the memory to set its own memory cycle time. If after sending an address out, the ìP dies not receive a READY input from memory, it enters a wait state for as long as the READY line is in 0 state. When the memory access is completed the READY goes high to indicate that the memory is ready for specified transfer.

109. List the four instructions which control the interrupt structure of the 8085 microprocessor.

DI (Disable Interrupts)

EI (Enable Interrupts)

RIM (Read Interrupt Masks)

SIM (Set Interrupt Masks)

110. What is meant by polling?

Polling or device polling is a process which identifies the device that has interrupted the microprocessor.

111. What is meant by interrupt?

Interrupt is an external signal that causes a microprocessor to jump to a specific subroutine.

112. Explain priority interrupts of 8085.

The 8085 microprocessor has five interrupt inputs. They are TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR. These interrupts have a fixed priority of interrupt service. If two or more interrupts go high at the same time, the 8085 will service them on priority basis. The TRAP has the highest priority followed by RST 7.5, RST 6.5, RST 5.5. The priority of interrupts in 8085 is shown in the table.

TRAP	1
RST 7.5	2
RST 6.5	3
RST 5.5	4
INTR	5

113. How many interrupts does 8085 have, mention them

The 8085 has 5 interrupt signals; they are INTR, RST7.5, RST6.5, RST5.5 and TRAP.

114. Basic concepts in memory interfacing

The primary function of memory interfacing is that the microprocessor should be able to read from and write into a given register of a memory chip. To perform these operations the microprocessor should

i. Be able to select the chip
ii. Identify the register
iii. Enable the appropriate buffer

115. What are the signals used in input control signal & output control signal in 8255?

Input control signal

i. STB (Strobe input)
ii. IBF (Input buffer full)
iii. INTR(Interrupt request)

Output control signal

i. OBF (Output buffer full)
ii. ACK (Acknowledge input)
iii. INTR(Interrupt request)

116. What are the features used mode 2 in 8255?

The single 8-bit port in-group A is available.

1)The 8-bit port is bi-directional and additionally a 5-bit control port is available.

2) Three I/O lines are available at port C, viz PC2-PC0.

3) Inputs and outputs are both latched.

4) The 5-bit control port C (PC3=PC7) is used for generating/accepting handshake signals for the 8-bit data transfer on port A.